



- ☐ Tentative Specification  
☐ Preliminary Specification  
☒ Approval Specification

**MODEL NO.: V420HK1****SUFFIX: PS5**

Ver. C7

**Customer:****APPROVED BY****SIGNATURE**

Name / Title \_\_\_\_\_

Note \_\_\_\_\_

\_\_\_\_\_

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Ken Wu	Peggi Chiu



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## REVISION HISTORY

Version	Date	Page(New)	Section	Description
Ver 2.0	Feb.,2,2012	All	All	The Approval specification was first issued.



## 1. GENERAL DESCRIPTION

### 1.1 OVERVIEW

V420HK1-PS5 is a 42" TFT Liquid Crystal Display product with driver ICs and 2ch-LVDS interface. This product supports 1920 x 1080 Full HDTV format and can display 16.7M colors(8-bit).

### 1.2 FEATURES

CHARACTERISTICS ITEMS	SPECIFICATIONS
Screen Diagonal [in]	42.02
Pixels [lines]	1920 × 1080
Active Area [mm]	930.24(H) × 523.26(V) (42" diagonal)
Sub-Pixel Pitch [mm]	0.1615(H) × 0.4845(V)
Pixel Arrangement	RGB vertical stripe
Weight [g]	TYP. 2155 g
Physical Size [mm]	946.24(W)X540.56(H)X1.75(D) Typ.
Display Mode	Transmissive mode / Normally black
Contrast Ratio	5000:1 Typ. (Typical value measure at CMI's module)
Glass thickness (Array / CF) [mm]	0.7 / 0.7
Viewing Angle (CR>20)	+88/-88(H), +88/-88(V) Typ. (CR ≥ 20) (Typical value measure at CMI's module)
Color Chromaticity	R=(0.662, 0.321) G=(0.265, 0.587) B= (0.135 ,0.099) W=(0.300, 0.347)  (Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages.)
Cell Transparency [%]	5%
Polarizer Surface Treatment	Anti-Glare coating (Haze 3.5 %), Hard coating (H)

### 1.3 MECHANICAL SPECIFICATIONS

Item	Min.	Typ.	Max.	Unit	Note
Weight		2155		g	
I/F connector mounting position	The mounting inclination of the connector makes the screen center within ± 0.5mm as the horizontal.				(1)

Note (1) Connector mounting position



## 2. ABSOLUTE MAXIMUM RATINGS

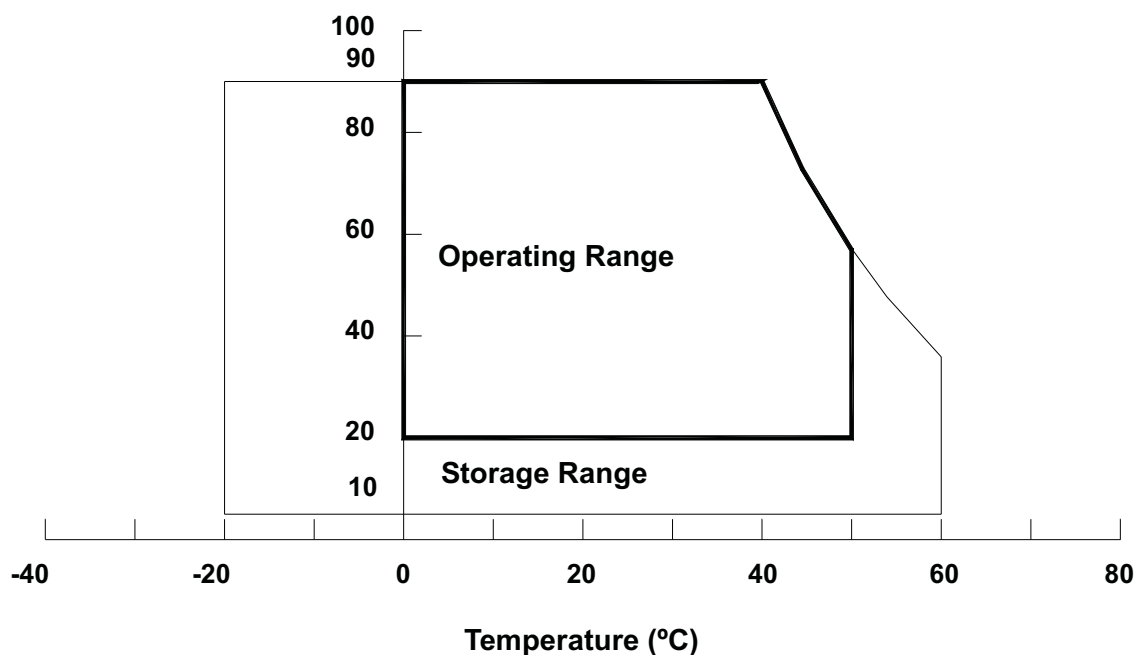
### 2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T <sub>ST</sub>	-20	+60	°C	(1)
Operating Ambient Temperature	T <sub>OP</sub>	0	+50	°C	(1), (2)

Note (1) Temperature and relative humidity range is shown in the figure below.

- (a) 90 %RH Max. ( $T_a \leq 40\text{ }^{\circ}\text{C}$ ).
- (b) Wet-bulb temperature should be 39 °C Max. ( $T_a > 40\text{ }^{\circ}\text{C}$ ).
- (c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 °C with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 °C. The range of operating temperature may degrade in case of improper thermal management in final product design.



### 2.2 PACKAGE STORAGE

When storing modules as spares for a long time, the following precaution is necessary.

- (a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.



(b)The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

## 2.3 ELECTRICAL ABSOLUTE RATINGS

### 2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V <sub>CC</sub>	-0.3	13.5	V	
Input Signal Voltage	V <sub>IN</sub>	-0.3	3.6	V	

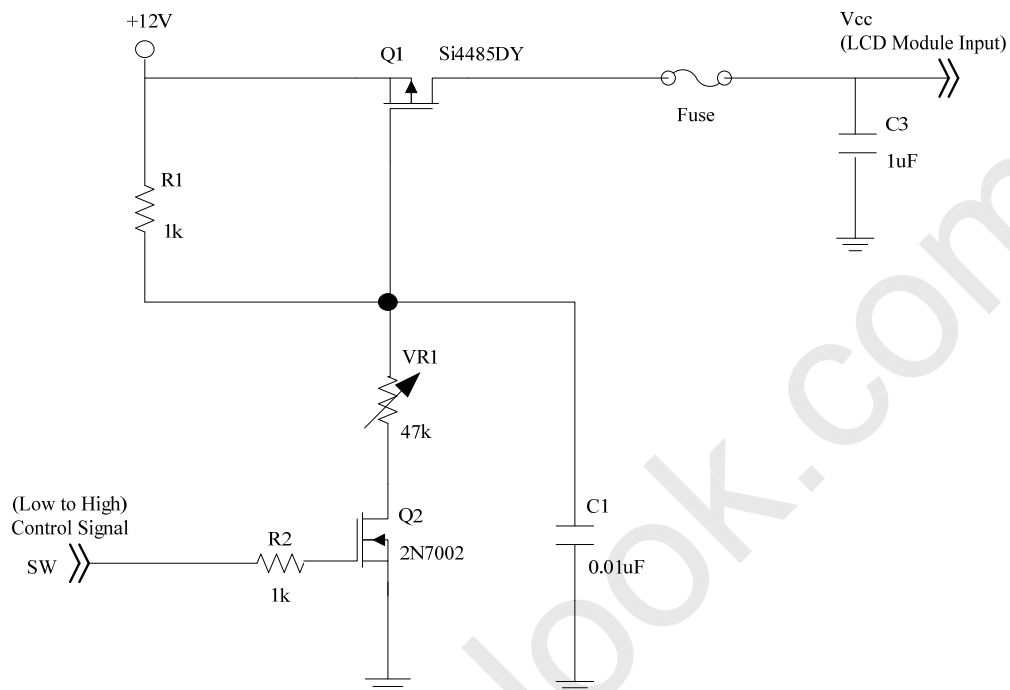
**3. ELECTRICAL CHARACTERISTICS****3.1 TFT LCD MODULE**

Ta = 25 ± 2 °C

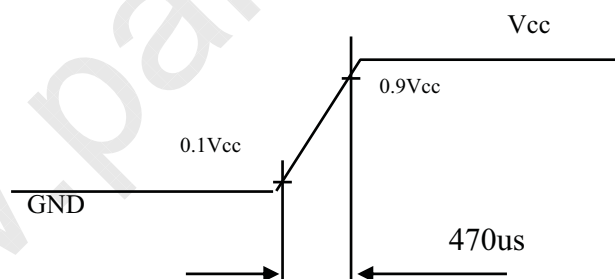
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V <sub>CC</sub>	10.8	12	13.2	V	(1)
Rush Current		I <sub>RUSH</sub>	-	-	2.6	A	(2)
Power Consumption	White Pattern	-		6.4	7.2	W	(3)
	Horizontal Stripe	-		12	14.4	W	
	Black Pattern	-		6.4	7.3	W	
Power Supply Current	White Pattern	-	-	0.53	0.6	A	
	Horizontal Stripe	-	-	1	1.2	A	
	Black Pattern	-	-	0.55	0.61	A	
LVDS interface	Differential Input High Threshold Voltage	V <sub>LVTH</sub>	+100	-	-	mV	(4)
	Differential Input Low Threshold Voltage	V <sub>LVTL</sub>	-	-	-100	mV	
	Common Input Voltage	V <sub>CM</sub>	1.0	1.2	1.4	V	
	Differential input voltage	V <sub>ID</sub>	200	-	600	mV	
	Terminating Resistor	R <sub>T</sub>	-	100	-	ohm	
CMOS interface	Input High Threshold Voltage	V <sub>IH</sub>	2.7	-	3.3	V	
	Input Low Threshold Voltage	V <sub>IL</sub>	0	-	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:



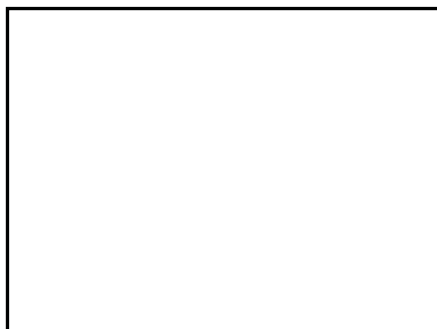
**Vcc rising time is 470us**





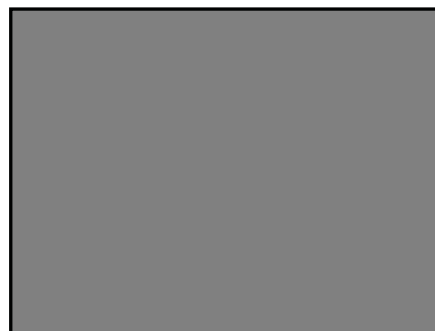
Note (3) The specified power consumption and power supply current is under the conditions at  $V_{CC} = 12\text{ V}$ ,  $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$ ,  $f_v = 120\text{ Hz}$ , whereas a power dissipation check pattern below is displayed.

a. White Pattern



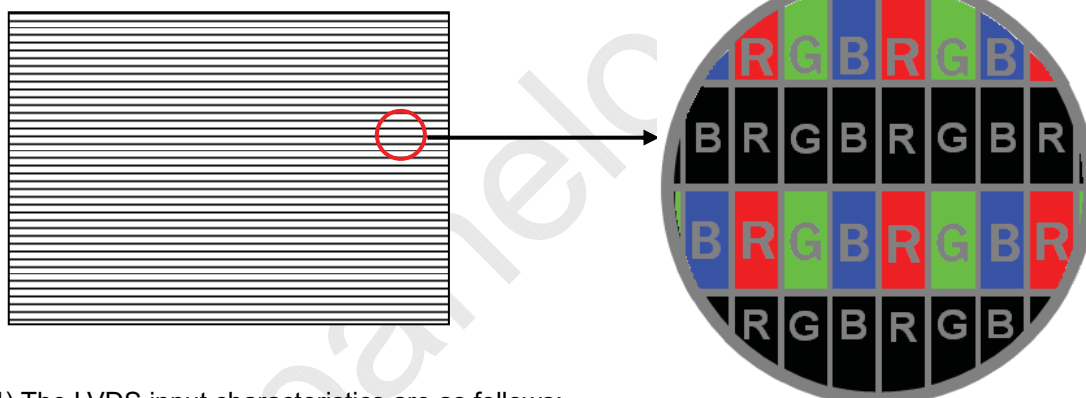
Active Area

b. Black Pattern

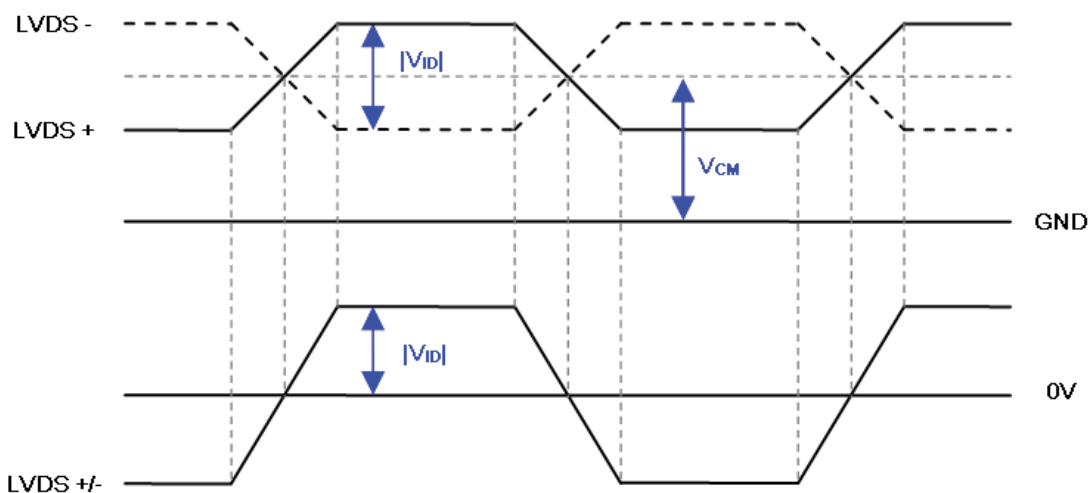


Active Area

c. Horizontal Stripe Pattern

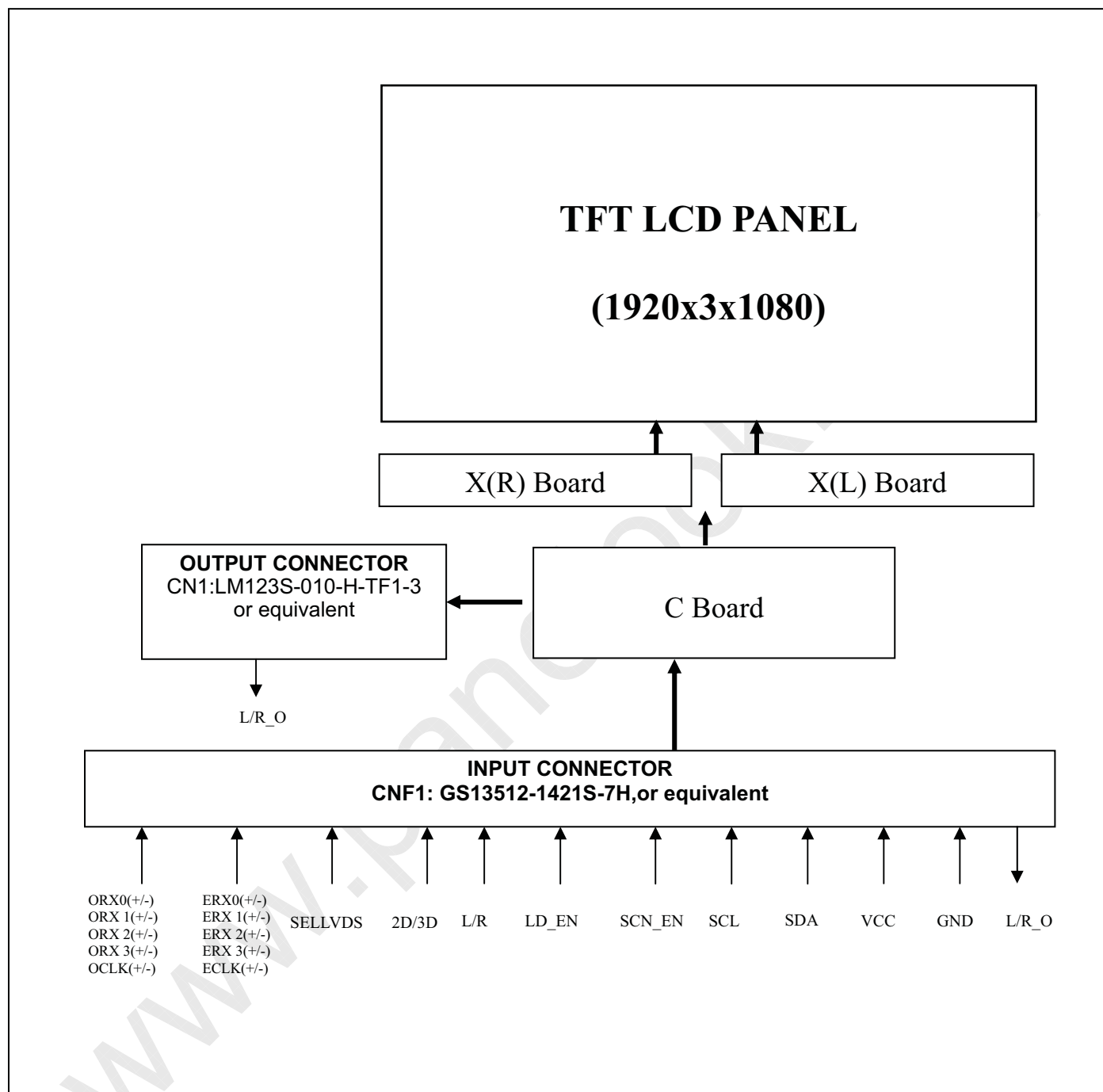


Note (4) The LVDS input characteristics are as follows:



## 4. BLOCK DIAGRAM OF INTERFACE

### 4.1 TFT LCD MODULE



**5. INTERFACE PIN CONNECTION****5.1 TFT LCD MODULE**

CNF1 Connector Pin Assignment: (GS13512-1421S-7H (FOXCONN) or equivalent)

Pin	Name	Description	Note
1	N.C.	No Connection	(1)
2	SCL	EEPROM Serial Clock (for local dimming demo function)	(11)
3	SDA	EEPROM Serial Data (for local dimming demo function)	
4	N.C.	No Connection	(1)
5	L/R_O	Output signal for Left Right Glasses control	(10)
6	N.C.	No Connection	(1)
7	SELLVDS	Input signal for LVDS Data Format Selection	(2)(7)
8	N.C.	No Connection	(1)
9	N.C.	No Connection	
10	N.C.	No Connection	
11	GND	Ground	
12	ORX0-	Odd pixel Negative LVDS differential data input. Channel 0	(9)
13	ORX0+	Odd pixel Positive LVDS differential data input. Channel 0	
14	ORX1-	Odd pixel Negative LVDS differential data input. Channel 1	
15	ORX1+	Odd pixel Positive LVDS differential data input. Channel 1	
16	ORX2-	Odd pixel Negative LVDS differential data input. Channel 2	
17	ORX2+	Odd pixel Positive LVDS differential data input. Channel 2	
18	GND	Ground	
19	OCLK-	Odd pixel Negative LVDS differential clock input	(9)
20	OCLK+	Odd pixel Positive LVDS differential clock input	
21	GND	Ground	
22	ORX3-	Odd pixel Negative LVDS differential data input. Channel 3	
23	ORX3+	Odd pixel Positive LVDS differential data input. Channel 3	(9)
24	N.C.	No Connection	
25	N.C.	No Connection	
26	2D/3D	Input signal for 2D/3D Mode Selection	(3)(6)(8)(12)
27	L/R	Input signal for Left Right eye frame synchronous	(4)(8)



28	ERX0-	Even pixel Negative LVDS differential data input. Channel 0	(9)
29	ERX0+	Even pixel Positive LVDS differential data input. Channel 0	
30	ERX1-	Even pixel Negative LVDS differential data input. Channel 1	
31	ERX1+	Even pixel Positive LVDS differential data input. Channel 1	
32	ERX2-	Even pixel Negative LVDS differential data input. Channel 2	
33	ERX2+	Even pixel Positive LVDS differential data input. Channel 2	
34	GND	Ground	
35	ECLK-	Even pixel Negative LVDS differential clock input.	(9)
36	ECLK+	Even pixel Positive LVDS differential clock input.	
37	GND	Ground	
38	ERX3-	Even pixel Negative LVDS differential data input. Channel 3	(9)
39	ERX3+	Even pixel Positive LVDS differential data input. Channel 3	
40	N.C.	No Connection	
41	N.C.	No Connection	
42	LD_EN	Input signal for Local Dimming Enable	(5)(8)
43	SCN_EN	Input signal for Scanning Enable	(6)(8)
44	GND	Ground	
45	GND	Ground	
46	GND	Ground	
47	N.C.	No Connection	
48	VCC	+12V power supply	
49	VCC	+12V power supply	
50	VCC	+12V power supply	
51	VCC	+12V power supply	

## CN1 Connector Pin Assignment (LM123S-010-H-TF1-3 (UNE) or equivalent)

1	N.C.	No Connection	(1)
2	N.C.	No Connection	
3	N.C.	No Connection	
4	GND	Ground	
5	N.C.	No Connection	(1)
6	L/R_O	Output signal for Left Right Glasses control	(10)
7	N.C.	No Connection	(1)
8	N.C.	No Connection	
9	N.C.	No Connection	
10	N.C.	No Connection	

Note (1) Reserved for internal use. Please leave it open.

Note (2) LVDS format selection.

L= Connect to GND, H=Connect to +3.3V or Open

SELLVDS	Note
L	JEIDA Format
H or Open	VESA Format

Note (3) 2D/3D mode selection.

L= Connect to GND or Open, H=Connect to +3.3V

2D/3D	Note
L or Open	2D Mode
H	3D Mode

Note (4) Input signal for Left Right eye frame synchronous

$V_{IL}=0\sim 0.7\text{ V}$ ,  $V_{IH}=2.7\sim 3.3\text{ V}$

L/R	Note
L	Right synchronous signal
H	Left synchronous signal

Note (5) Local dimming enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

LD_EN	Note
L	Local Dimming Disable
H or Open	Local Dimming Enable

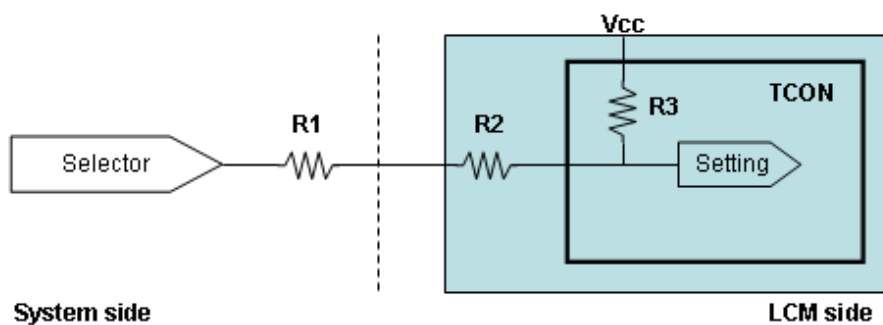
Note (6) Scanning enable selection.

L= Connect to GND or Open, H=Connect to +3.3V

SCN_EN	Note
L or Open	Scanning Disable
H	Scanning Enable

Note (7) SELLVDS, LD\_EN signal pin connected to the LCM side has the following diagram.

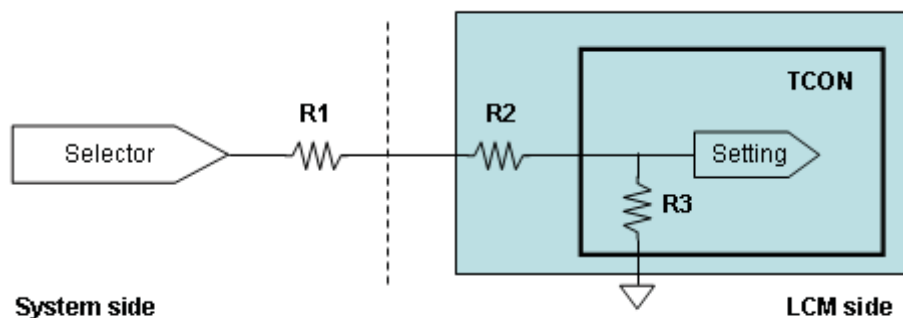
R1 in the system side should be less than 1K Ohm. ( $R1 < 1K \text{ Ohm}$ )



System side  
 $R1 < 1K$

Note (8) 2D/3D, L/R and SCN\_EN signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. ( $R1 < 1K \text{ Ohm}$ )



System side:  $R1 < 1K$

Note (9) Two pixel data send into the module for every clock cycle. The first pixel of the frame is odd pixel and the second pixel is even pixel.

Note (10) The definition of L/R\_O signal as follows

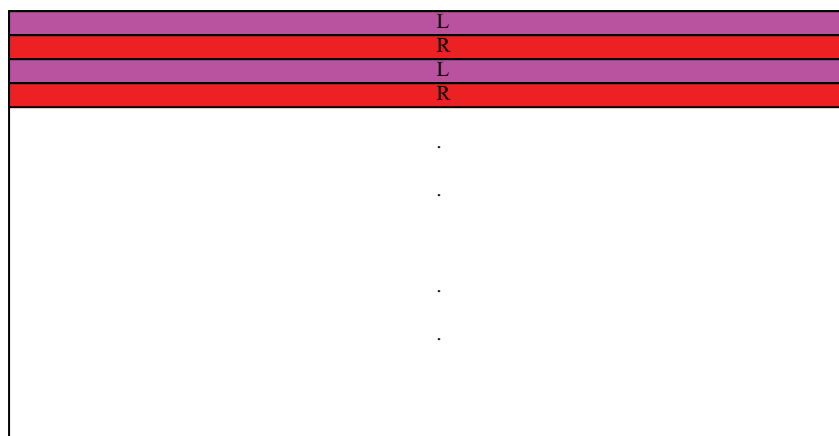
L= 0V , H= +3.3V

L/R_O	Note
L	Right glass turn on
H	Left glass turn on



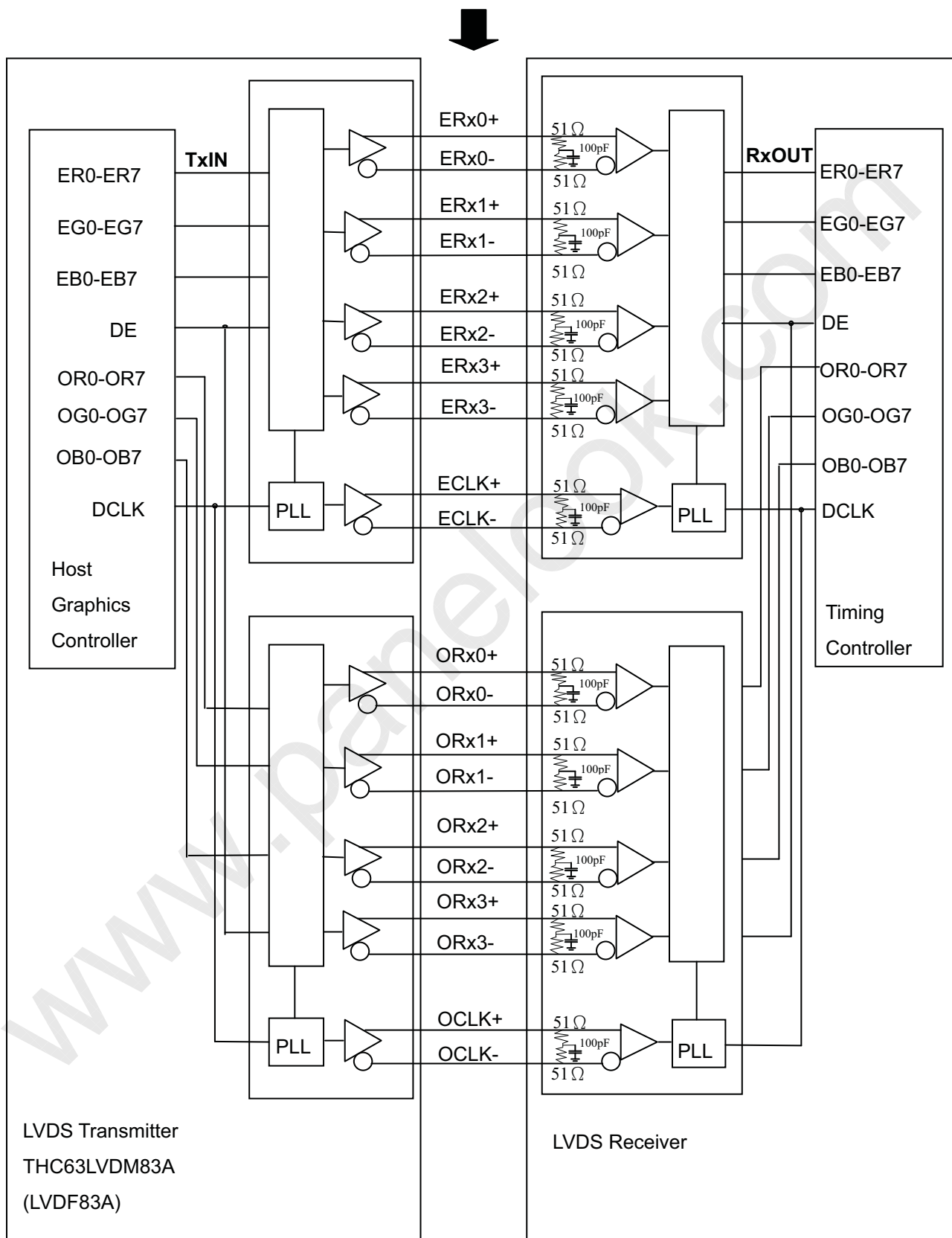
Note (11) Please reference Appendix A

Note (12) Currently, we only support line alternative format (1st line is left signal), show as the attached block diagram. In the future, we will support other format.



Line alternative format

## 5.2 BLOCK DIAGRAM OF INTERFACE







ER0~ER7: Even pixel R data

EG0~EG7: Even pixel G data

EB0~EB7: Even pixel B data

OR0~OR7: Odd pixel R data

OG0~OG7: Odd pixel G data

OB0~OB7: Odd pixel B data

DE: Data enable signal

DCLK: Data clock signal

Notes (1) The system must have the transmitter to drive the module.

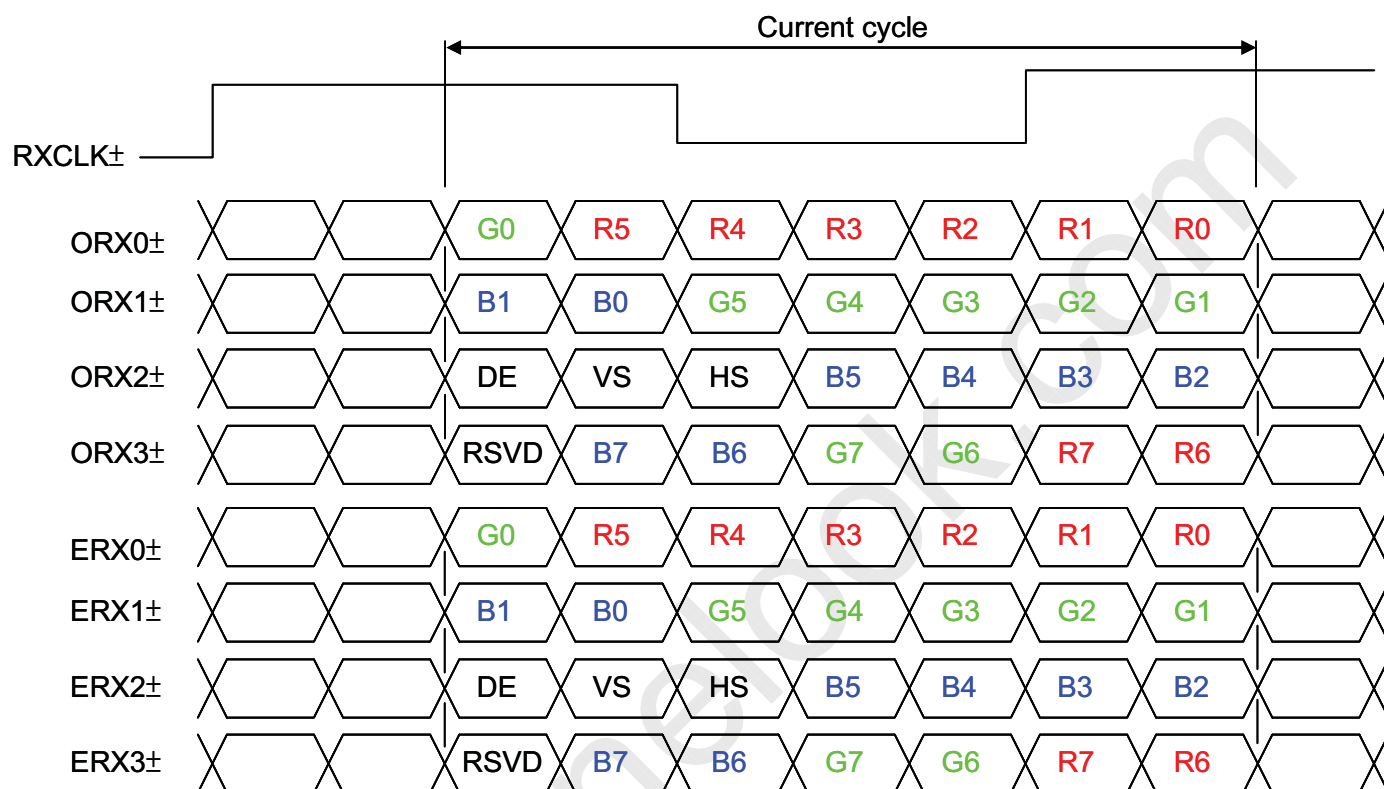
Notes (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

### 5.3 LVDS INTERFACE

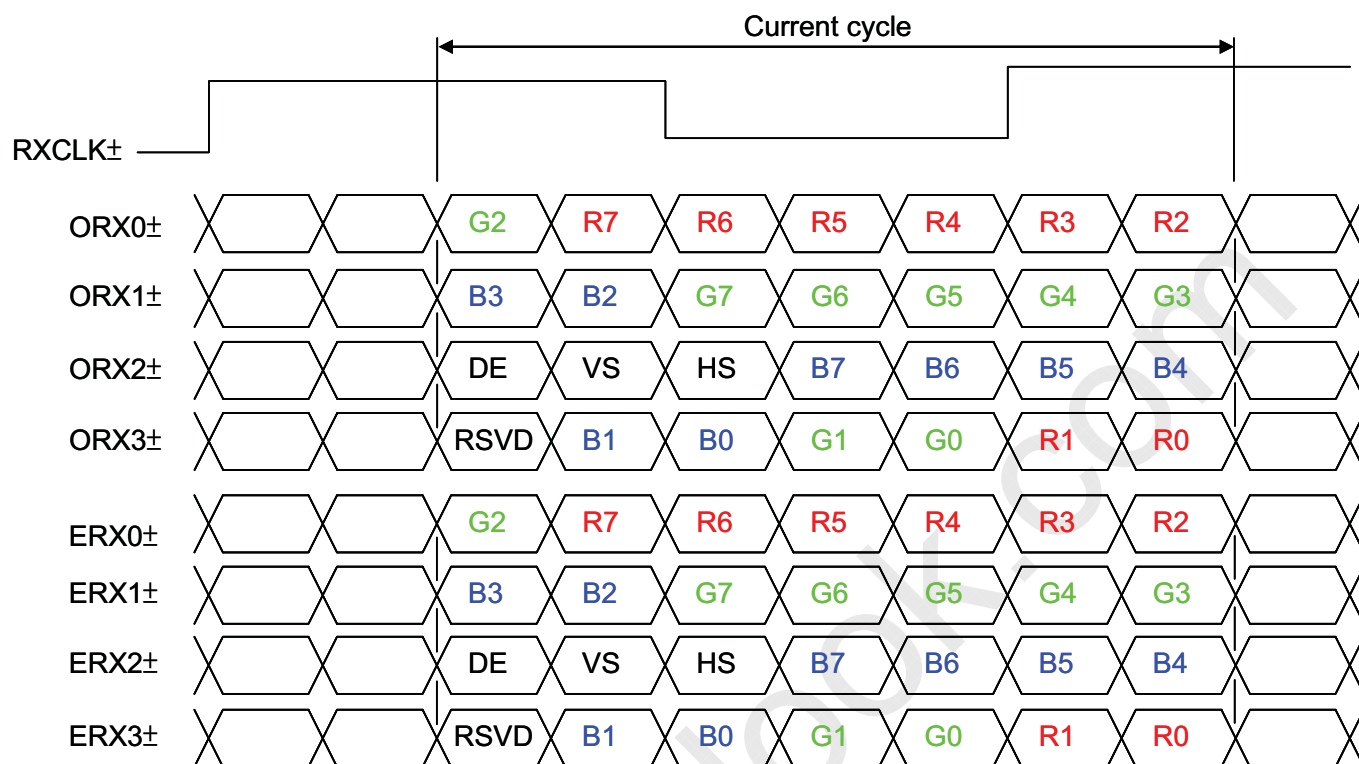
JEIDA Format : SELLVDS = L

VESA Format : SELLVDS = H or Open

VESA LVDS format:



JEDIA LVDS format:



R0~R7: Pixel R Data (7; MSB, 0; LSB)

G0~G7: Pixel G Data (7; MSB, 0; LSB)

B0~B7: Pixel B Data (7; MSB, 0; LSB)

DE : Data enable signal

DCLK : Data clock signal

Notes: (1) RSVD (reserved) pins on the transmitter shall be "H" or "L".

**5.4 COLOR DATA INPUT ASSIGNMENT**

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of the color versus data input.

Color		Data Signal																															
		Red										Green										Blue											
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0		
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Gray Scale Of Red	Red (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Red (2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	:																																
	:																					;											
	Red (1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red (1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	
	Green (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
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	Green (1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green (1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Green (1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue (0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
	Blue (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
	Blue (2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	
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	Blue (1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	1	

Blue (1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
Blue (1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

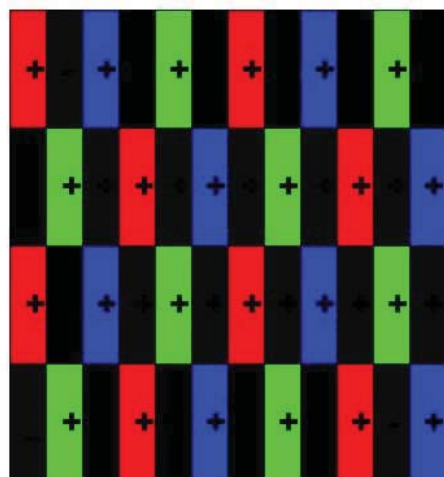
Note (1) 0: Low Level Voltage, 1: High Level Voltage

## 5.5 FLICKER (Vcom) ADJUSTMENT

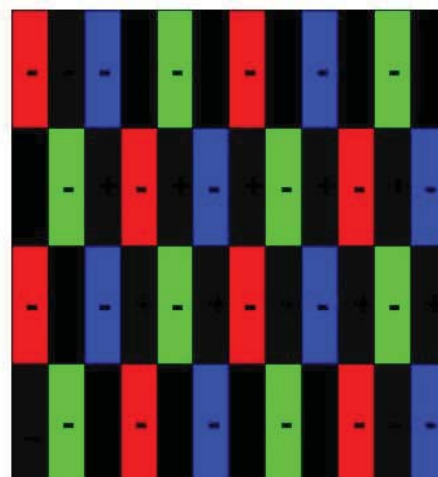
### (1) Adjustment Pattern:

Flicker pattern was shown as below. If customer need below pattern, please directly contact with Account FAE.

Frame N



Frame N+1



### (2) Adjustment method: (Digital V-com)

Programmable memory IC is used for Digital V-com adjustment in this model. CMI provide Auto Vcom tools to adjust Digital V-com. The detail connection and setting instruction, please directly contact with Account FAE or refer CMI Auto V-com adjustment OI.



## 6. INTERFACE TIMING

### 6.1 INPUT SIGNAL TIMING SPECIFICATIONS (Ta = 25 ± 2 °C)

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	$F_{clkin}$ (=1/TC)	60	74.25	77	MHz	
	Input cycle to cycle jitter	$T_{rcl}$	-	-	200	ps	(3)
	Spread spectrum modulation range	$F_{clkin\_mod}$	$F_{clkin}-2\%$	-	$F_{clkin}+2\%$	MHz	(4)
	Spread spectrum modulation frequency	$F_{SSM}$	-	-	200	KHz	
LVDS Receiver Data	Receiver Skew Margin	$T_{RSKM}$	-400	—	400	ps	(5)

#### 6.1.1 Timing spec for Frame Rate = 100Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		$F_{r5}$	47	50	53	Hz	
	3D mode		$F_{r5}$	50	50	50	Hz	(7)
Vertical Active Display Term	2D Mode	Total	$T_v$	1115	1125	1380	Th	$T_v=T_{vd}+T_{vb}$
		Display	$T_{vd}$	1080	1080	1080	Th	—
		Blank	$T_{vb}$	35	45	300	Th	—
	3D Mdoe	Total	$T_v$	1350			Th	(6)(8)
		Display	$T_{vd}$	1080			Th	
		Blank	$T_{vb}$	270			Th	
Horizontal Active Display Term	2D Mode	Total	$T_h$	1050	1100	1150	Tc	$T_h=T_{hd}+T_{hb}$
		Display	$T_{hd}$	960	960	960	Tc	—
		Blank	$T_{hb}$	90	140	190	Tc	—
	3D Mdoe	Total	$T_h$	1050	1100	1150	Tc	$T_h=T_{hd}+T_{hb}$
		Display	$T_{hd}$	960	960	960	Tc	—
		Blank	$T_{hb}$	90	140	190	Tc	—



## 6.1.2 Timing spec for Frame Rate = 120Hz

Signal	Item		Symbol	Min.	Typ.	Max.	Unit	Note
Frame rate	2D mode		F <sub>r6</sub>	57	60	62.5	Hz	
	3D mode		F <sub>r6</sub>	60	60	60	Hz	(7)
Vertical Active Display Term	2D Mode	Total	T <sub>v</sub>	1115	1125	1380	Th	T <sub>v</sub> =T <sub>vd</sub> +T <sub>v</sub> b
		Display	T <sub>vd</sub>	1080	1080	1080	Th	—
		Blank	T <sub>vb</sub>	35	45	300	Th	—
	3D Mdoe	Total	T <sub>v</sub>	1125			Th	(6)(8)
		Display	T <sub>vd</sub>	1080			Th	
		Blank	T <sub>vb</sub>	45			Th	
Horizontal Active Display Term	2D Mode	Total	T <sub>h</sub>	1050	1100	1150	T <sub>c</sub>	T <sub>h</sub> =T <sub>hd</sub> +T <sub>h</sub> b
		Display	T <sub>hd</sub>	960	960	960	T <sub>c</sub>	—
		Blank	T <sub>hb</sub>	90	140	190	T <sub>c</sub>	—
	3D Mdoe	Total	T <sub>h</sub>	1050	1100	1150	T <sub>c</sub>	T <sub>h</sub> =T <sub>hd</sub> +T <sub>h</sub> b
		Display	T <sub>hd</sub>	960	960	960	T <sub>c</sub>	—
		Blank	T <sub>hb</sub>	90	140	190	T <sub>c</sub>	—

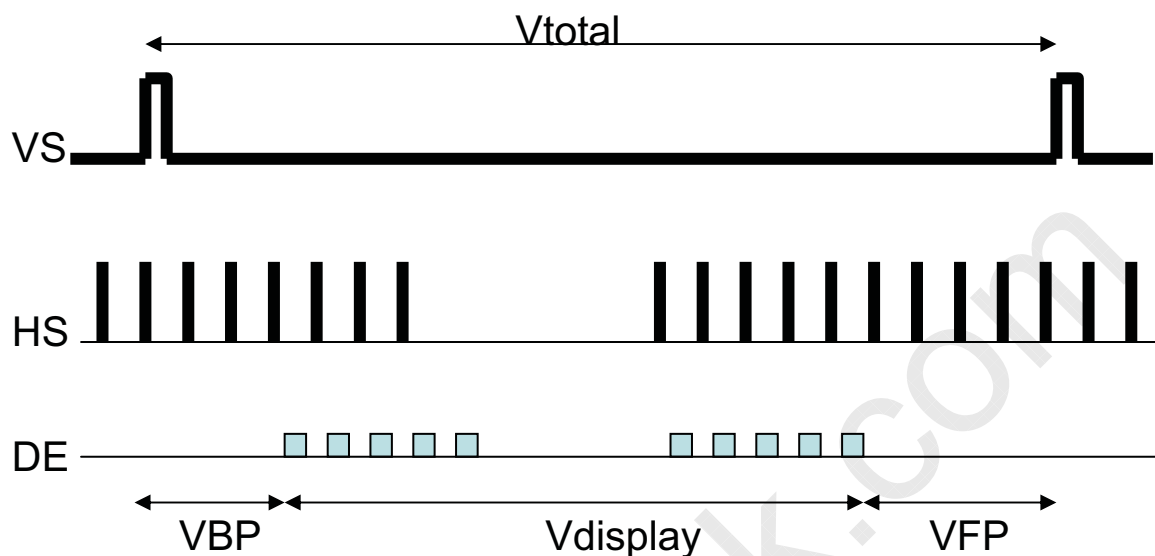
Note (1) Please make sure the range of pixel clock has follow the below equation:

$$F_{clkin(max)} \geq F_{r6} \times T_v \times T_h$$

$$F_{r5} \times T_v \times T_h \geq F_{clkin(min)}$$



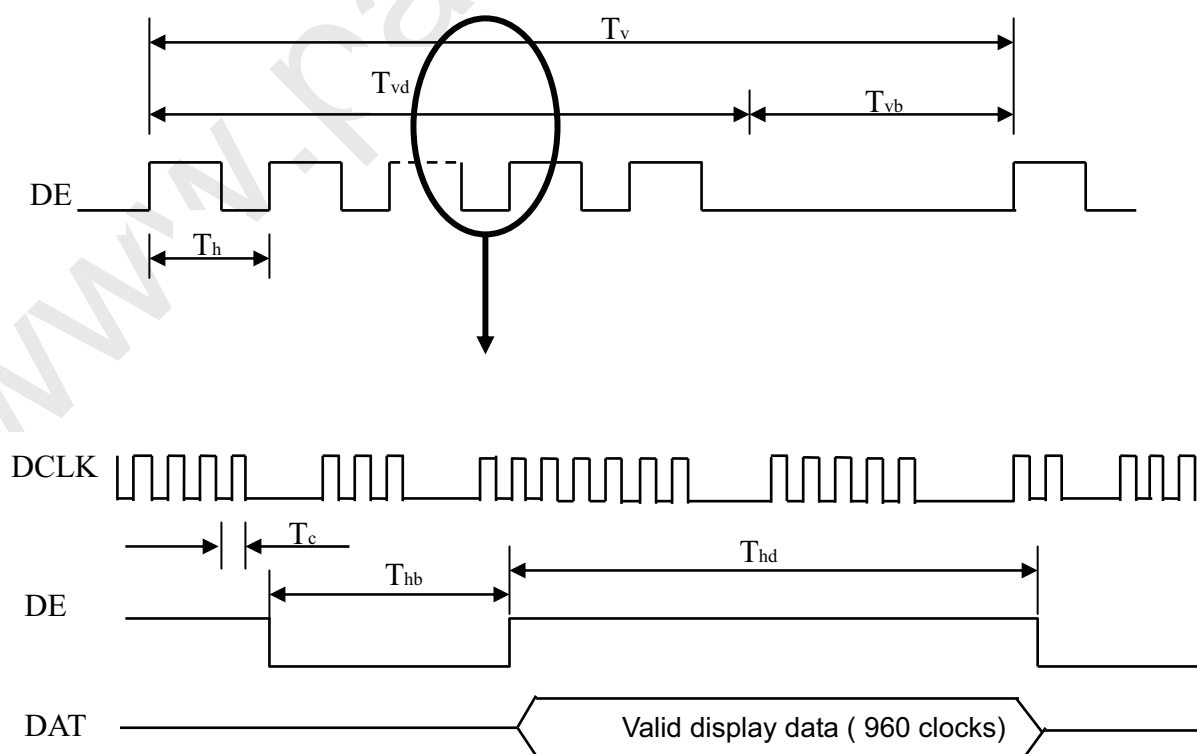
## INPUT SIGNAL TIMING DIAGRAM



- VBP max : 150 line

Suggest  $VBP = VFP = \frac{1}{2} * (V_{total} - V_{display})$

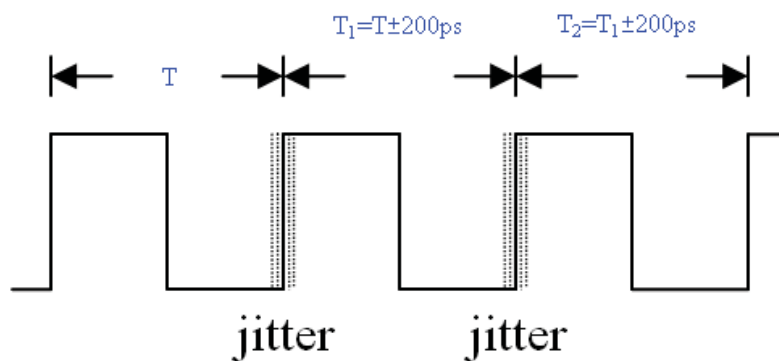
Note (2) DE timing:



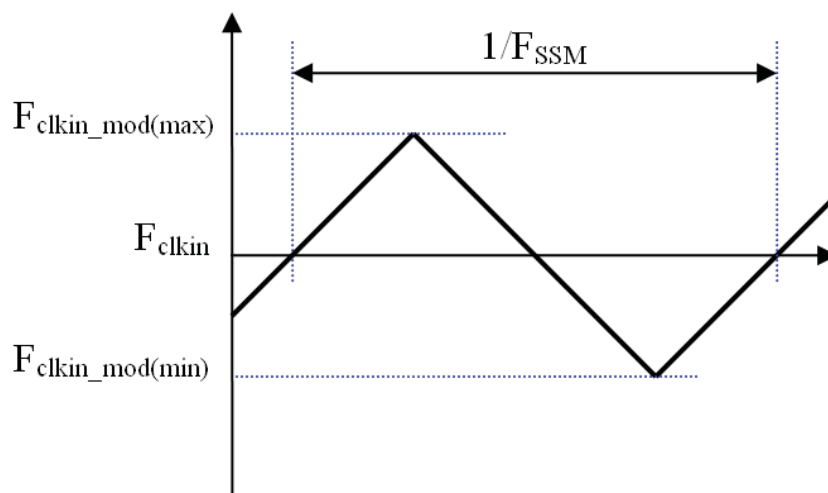




Note (3) The input clock cycle-to-cycle jitter is defined as below figures.  $Trcl = |T_1 - T_1|$

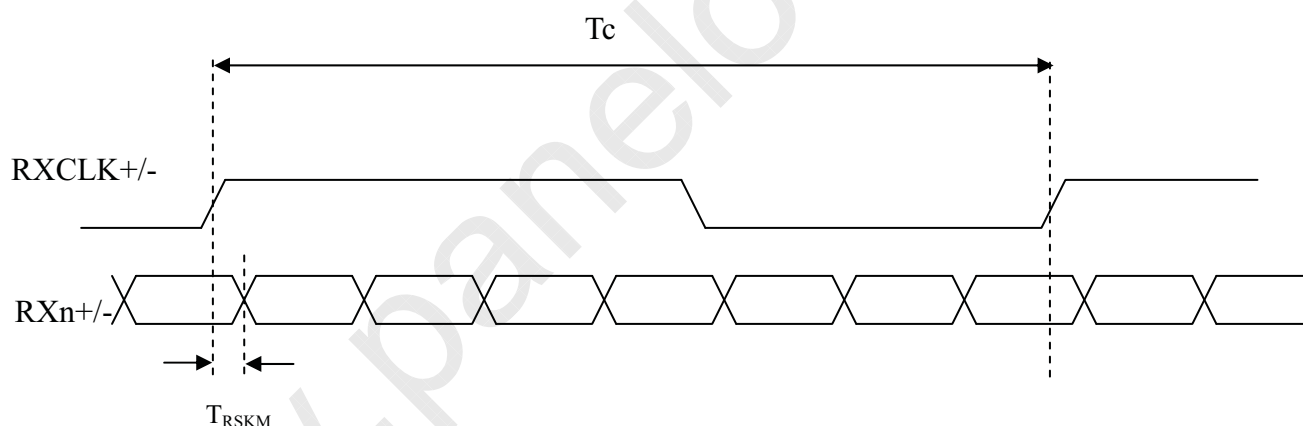


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

## LVDS RECEIVER INTERFACE TIMING DIAGRAM



Note (6) Please fix the Vertical timing (Vertical Total =1350 / Display =1080 / Blank = 270) in 50Hz 3D mode and Vertical timing (Vertical Total =1125 / Display =1080 / Blank = 45) in 60Hz 3D mode

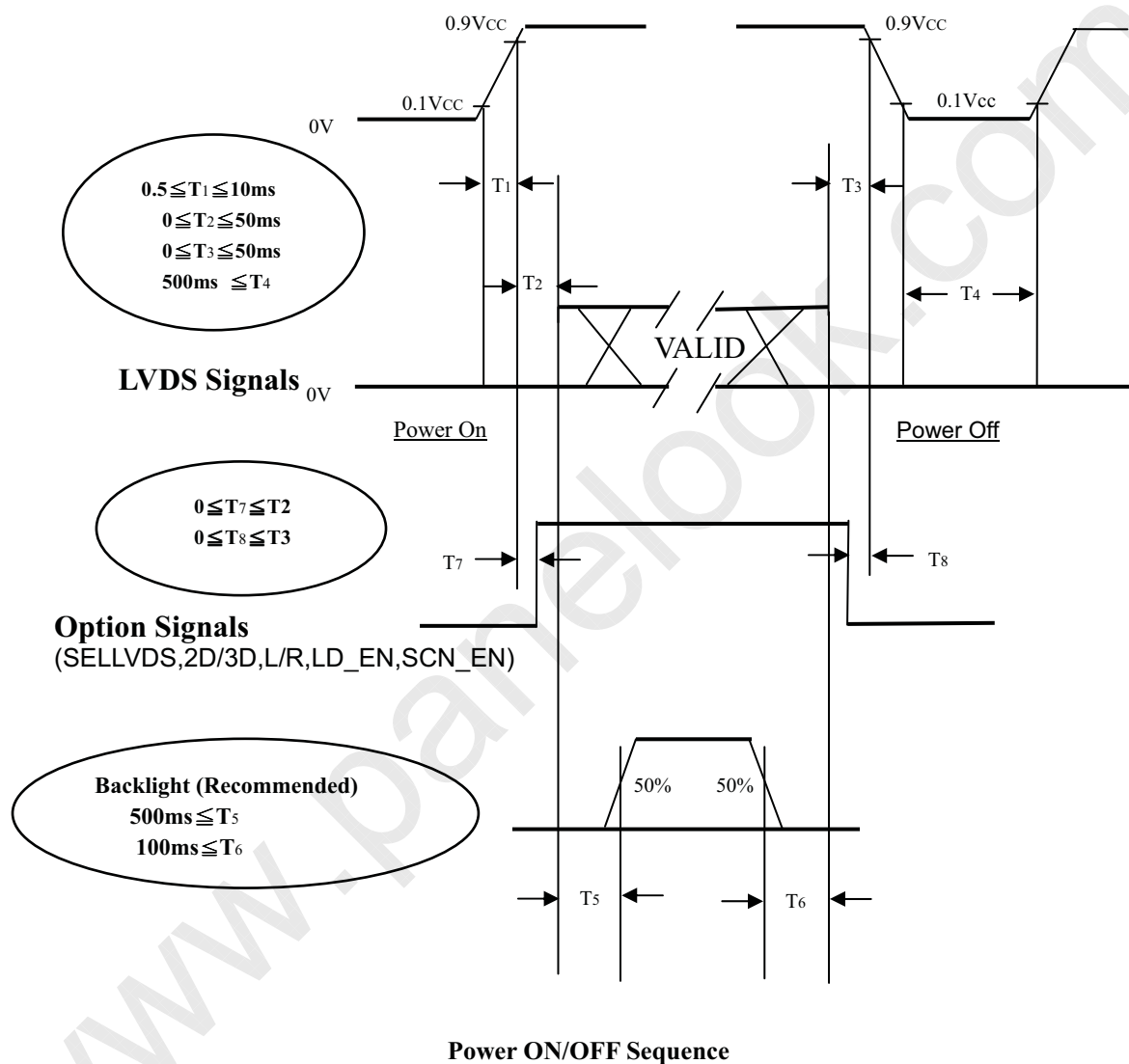
Note (7) In 3D mode, the set up Fr5 and Fr6 in Typ.  $\pm 3$  HZ .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

Note (8) In 3D mode, the set up Tv and Tvb in Typ.  $\pm 30$ .In order to ensure that the electric function performance to avoid no display symptom.(Except picture quality symptom.)

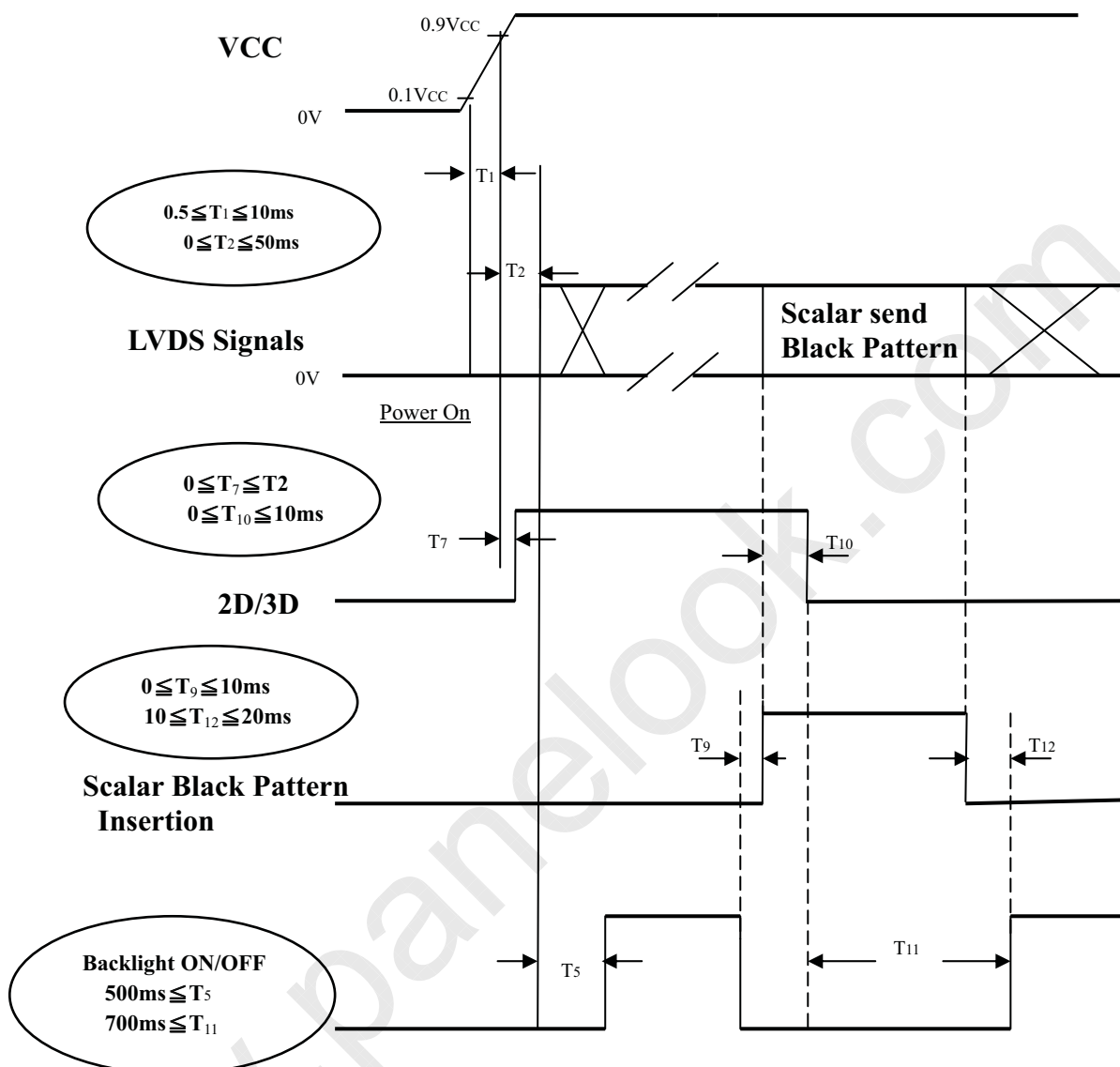
## 6.2 POWER ON/OFF SEQUENCE

### 6.2.1 POWER ON/OFF SEQUENCE ( $T_a = 25 \pm 2^\circ\text{C}$ )

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



## 6.2.2 2D/3D MODE CHANGE SIGNAL SEQUENCE WITHOUT VCC TURN OFF AND TURN ON



Note (1) The supply voltage of the external system for the module input should follow the definition of V<sub>cc</sub>.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of V<sub>cc</sub> is in off level, please keep the level of input signals on the low or high impedance. If T<sub>2</sub><0, that maybe cause electrical overstress failure.

Note (4) T<sub>4</sub> should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

Note (6) When 2D/3D mode is changed, TCON will insert black pattern internally. During black insertion, TCON would load required optical table and TCON parameter setting. The black insertion time should be longer than 650ms because TCON must recognize 2D or 3D format and set the correct parameter.

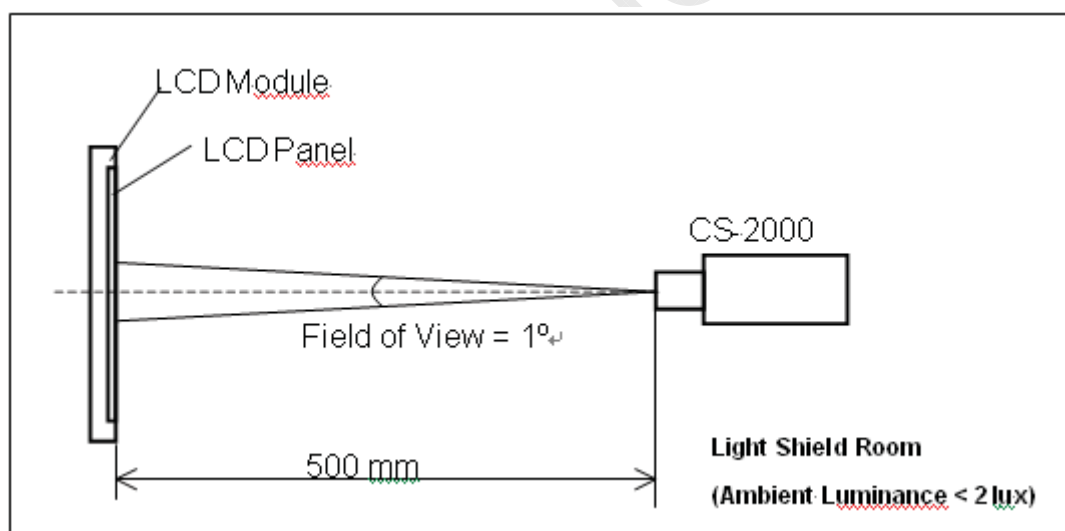
## 7. OPTICAL CHARACTERISTICS

### 7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	℃
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	VCC	12	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Current	IL	120	mA
Vertical Frame Rate	Fr	120	Hz

Local Dimming Function should be Disable before testing to get the steady optical characteristics  
(According to 5.1 CNF1 Connector Pin Assignment, Pin no. "42")

The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring in a windless room.





## 7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in 7.1.

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR			5000	-	-	(2), (4)
Response Time		Gray to gray	$\theta_x=0^\circ, \theta_Y=0^\circ$ With CMI Module	-	6	12	ms	(5)
Center Transmittance		T%		-	5	-	%	(2), (7)
White Variation		$\delta W$		-	-	1.3	-	(2), (6)
Color Chromaticity	Red	Rcx	$\theta_x=0^\circ, \theta_Y=0^\circ$ CS-2000 Standard light source “C”	Typ - 0.03	0.662	Typ + 0.03	-	Color Chromaticity
		Rcy			0.321		-	
	Green	Gcx			0.265		-	
		Gcy			0.587		-	
	Blue	Bcx			0.135		-	
		Bcy			0.099		-	
	White	Wcx			0.300		-	
		Wcy			0.347		-	
	Viewing Angle	Horizontal			$\theta_x+$		$CR\geq 20$ With CMI Module	
$\theta_x-$			80	88	-			
Vertical		$\theta_Y+$	80	88	-			
		$\theta_Y-$	80	88	-			
Transmission direction of the up polarizer		$\Phi_{up-P}$	-	-	90	-	Deg.	(8)
Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note

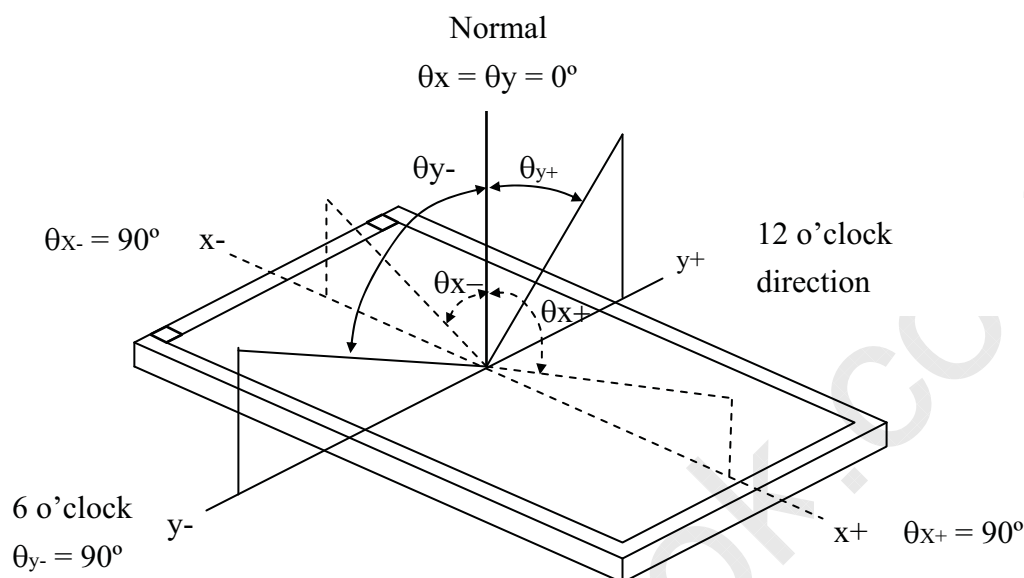
Note (1) Light source is the standard light source "C" which is defined by CIE and driving voltages are based on suitable gamma voltages. The calculating method is as following :

1. Measure Module's and BLU's spectrums. W, R, G, B are with signal input. BLU(for V420HK1\_LS5 502) is supplied by CMI.
2. Calculate cell's spectrum.
3. Calculate cell's chromaticity by using the spectrum of standard light source "C"

Note (2) Light source is the BLU which is supplied by CMI and driving voltages are based on suitable gamma voltages.

Note (3) Definition of Viewing Angle ( $\theta_x, \theta_y$ ):

Viewing angles are measured by Conoscope Cono-80 ( or Eldim EZ-Contrast 160R )



Note (4) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

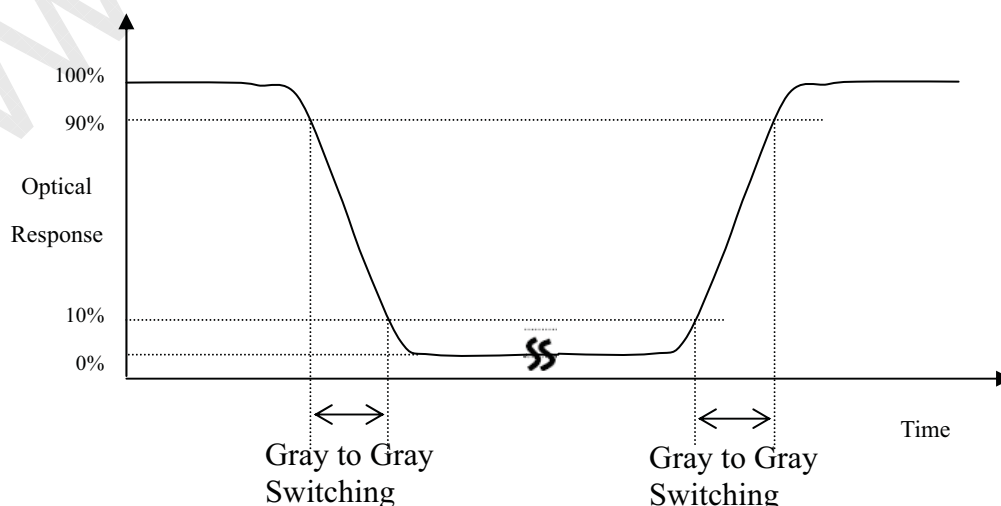
$$\text{Contrast Ratio (CR)} = L_{255} / L_0$$

L 255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (1), where CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (6).

Note (5) Definition of Gray to Gray Switching Time:



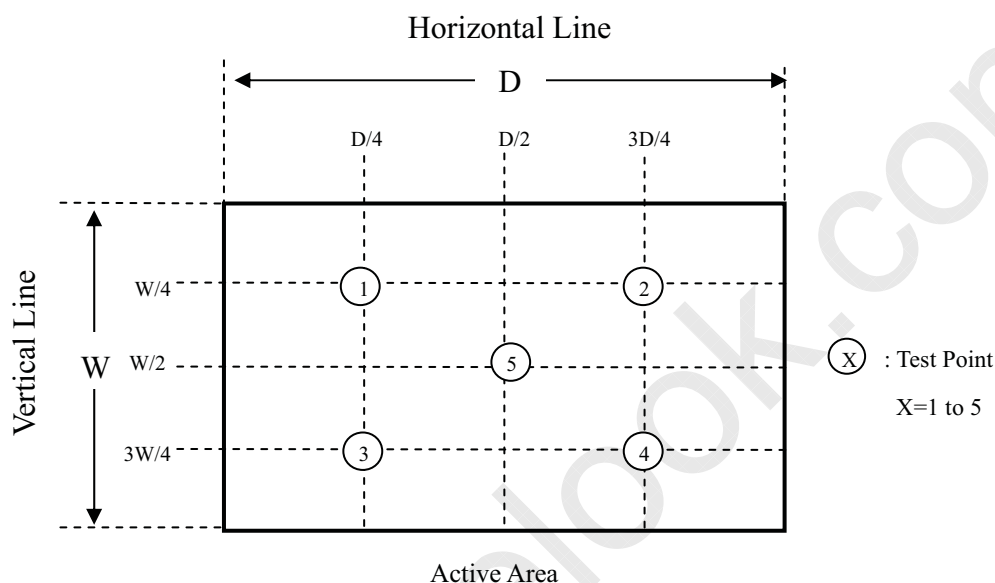
The driving signal means the signal of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Gray to gray average time means the average switching time of gray level 0, 124, 252, 380, 508, 636, 764, 892 and 1023.

Note (6) Definition of White Variation ( $\delta W$ ):

Measure the luminance of gray level 255 at 5 points

$$\delta W = \text{Maximum [L (1), L (2), L (3), L (4), L (5)]} / \text{Minimum [L (1), L (2), L (3), L (4), L (5)]}$$



Note (7) Definition of Transmittance ( $T\%$ ):

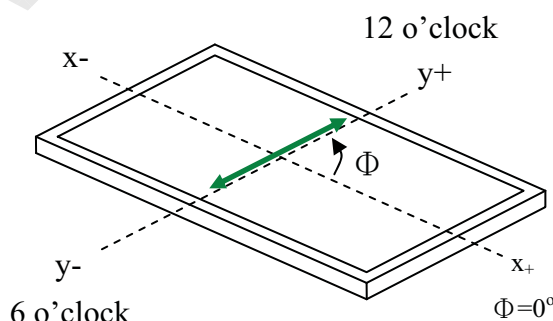
Measure the luminance of gray level 255 at 5 points of LCD module.

$$\text{Transmittance (T\%)} = \frac{\text{average [L (1), L (2), L (3), L (4), L (5)] of LCD module}}{\text{average [L (1), L (2), L (3), L (4), L (5)] of backligh unit}} \times 100\%$$

The 5 point is corresponding of the point X at the figure in Note (5).

Note (8) This is a reference for designing the shutter glasses of 3D application. (VA case)

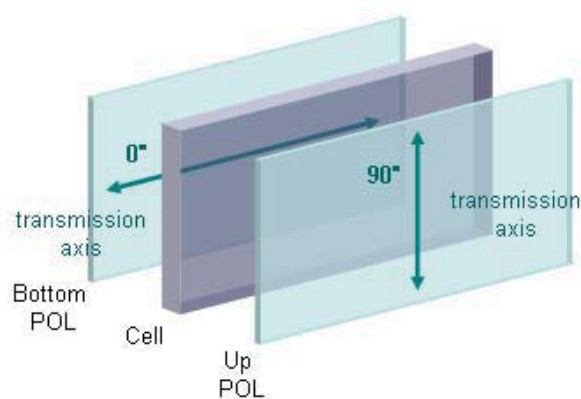
Definition of the transmission direction of the up polarizer ( $\Phi_{\text{up-P}}$ ) on LCD Module:



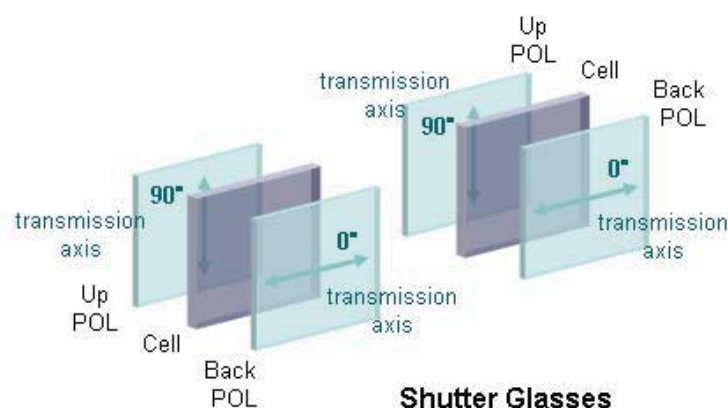
**Up Polarizer**



The transmission axis of the front polarizer of the shutter glasses should be parallel to this panel transmission direction to get a maximum 3D mode luminance.



**LCD Module**

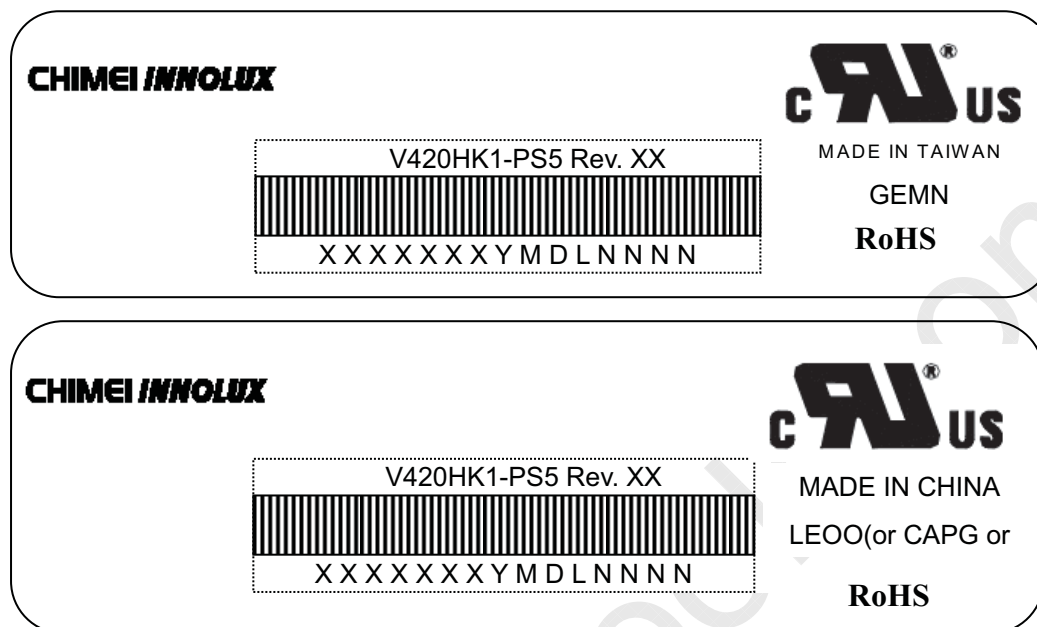


**Shutter Glasses**

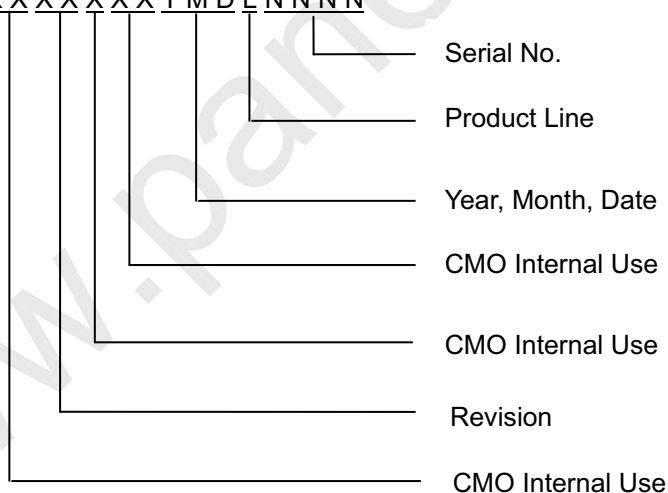
## 8. DEFINITION OF LABELS

### 8.1 CMI MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: V420HK1-PS5  
 (b) Revision: Rev. XX, for example: A0, A1... B1, B2... or C1, C2...etc.  
 (c) Serial ID: XXXXXXXXYMDLNNNN



Serial ID includes the information as below:

- (a) Manufactured Date: Year: 2001=1, 2002=2, 2003=3, 2004=4....2010=0, 2011=1, 2012=2....  
 Month: 1~9, A~C, for Jan. ~ Dec.  
 Day: 1~9, A~Y, for 1<sup>st</sup> to 31<sup>st</sup>, exclude I ,O, and U.  
 (b) Revision Code: Cover all the change  
 (c) Serial No.: Manufacturing sequence of product  
 (d) Product Line: 1 -> Line1, 2 -> Line 2, ...etc.

## 9. PACKAGING

### 9.1 PACKING SPECIFICATIONS

- (1) 10 LCD TV Panels / 1 Box
- (2) Box dimensions : 1110 (L) X 810 (W) X99 (H)mm
- (3) Weight : approximately 27Kg ( 10 panels per box)
- (4) 120 LCD TV Panels / 1 Group

### 9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

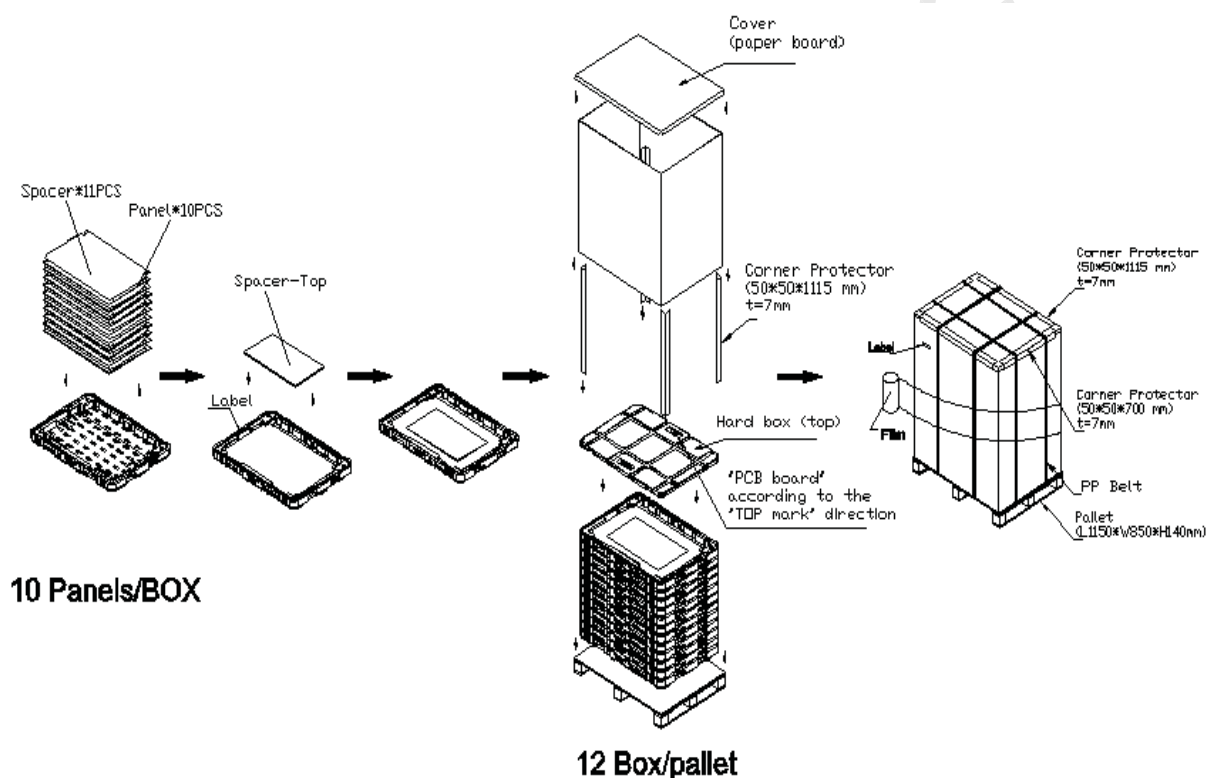
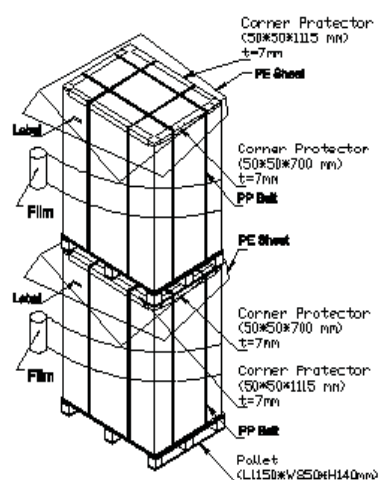


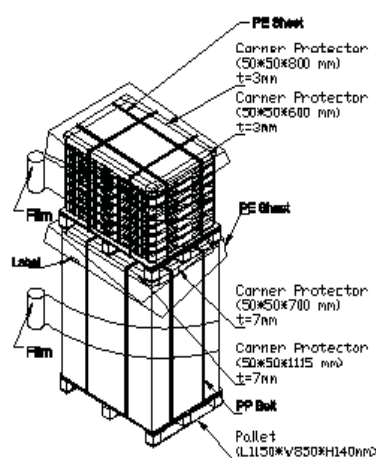
Figure.9-1 packing method

## Sea & Land Transportation (40ft HQ Container)



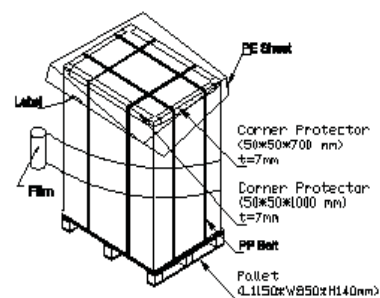
(12 Box / Pallet) + (12 Box / Pallet)

## Sea & Land Transportation



(12 Box / Pallet) + (8 Box / Pallet)

## Air Transportation



12 Box / Pallet

Figure.9-2 packing method



## 10. INTERNATIONAL STANDARD

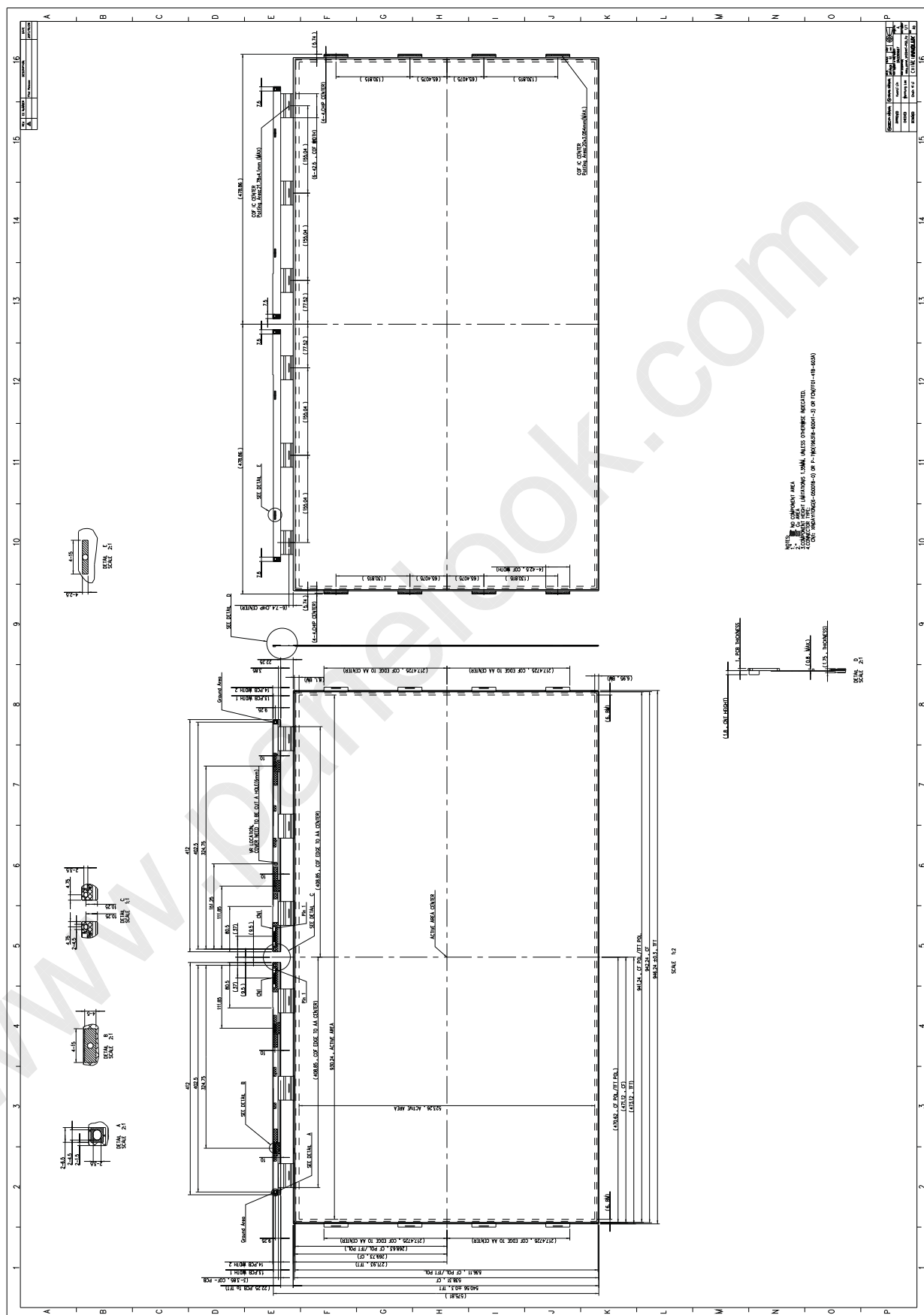
### 10.1 ASSEMBLY AND HANDLING PRECAUTIONS

- [ 1 ] Do not apply rough force such as bending or twisting to the module during assembly.
- [ 2 ] It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.
- [ 3 ] Do not apply pressure or impulse to the module to prevent the damage of LCD panel and Backlight.
- [ 4 ] Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.
- [ 5 ] The distance between COF edge and rib of BLU must bigger than 5mm. This can prevent the damage of COF when assemble the module.
- [ 6 ] Do not design sharp-pointed structure / parting line / tooling gate on the COF position of plastic parts, because the burr will scrape the COF.
- [ 7 ] If COF would bended to assemble in the module. Do not put the IC location on the bending corner of COF.
- [ 8 ] The gap between COF IC and any structure of BLU must bigger than 2mm. This can prevent the damage of COF IC
- [ 9 ] Bezel opening must have no burr. Burr will scrape the panel surface.
- [ 10 ] Bezel of module and bezel of set can not press or touch the panel surface. It will make light leakage or scrape.
- [ 11 ] When module used FFC / FPC, but no FFC / FPC to be attached in the open cell. Customer can refer the FFC / FPC drawing and buy it by self.
- [ 12 ] The gap between Panel and any structure of Bezel must bigger than 2mm. This can prevent the damage of Panel.
- [ 13 ] Do not plug in or pull out the I/F connector while the module is in operation.
- [ 14 ] Do not disassemble the module.
- [ 15 ] Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.
- [ 16 ] Moisture can easily penetrate into LCD module and may cause the damage during operation.
- [ 17 ] When storing modules as spares for a long time, the following precaution is necessary.
  - [ 17.1 ] Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35°C at normal humidity without condensation.
  - [ 17.2 ] The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.
- [ 18 ] When ambient temperature is lower than 10°C, the display quality might be reduced.

**10.2 SAFETY PRECAUTIONS**

- [ 1 ] The startup voltage of a Backlight is approximately 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the Backlight unit.
- [ 2 ] If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.
- [ 3 ] After the module's end of life, it is not harmful in case of normal operation and storage.

## 11. MECHANICAL CHARACTERISTICS



**Appendix A. Local Dimming demo function****A.1 I2C address and write command**

Device address: 0xe0

Register address: 0x65

Command data: 0x16 0x00 0x00 0x00 0x00 0x00: Local Dimming demo mode OFF (Note 1)

0x16 0x00 0x00 0x00 0x00 0x01: Local Dimming demo mode ON (Demo in right half screen)

(Note 2)

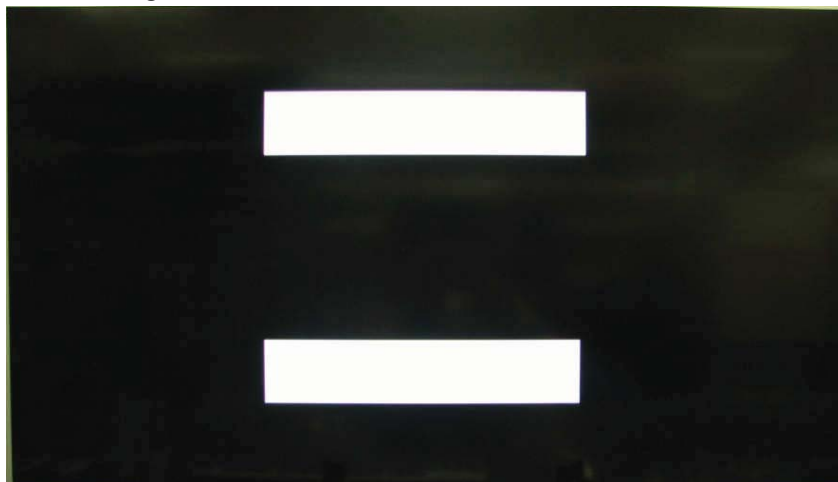
Preamble data: 0x26 0x38

I2C data:

Device Address			Preamble data		Preamble data	
START	11100000 (0xE0)	ACK	00100110 (0x26)	ACK	00111000 (0x38)	ACK
Register Address		Command Data		Command Data		
01100101 (0x65)	ACK	00010110 (0x16)	ACK	00000000 (0x00)	ACK	
Command Data		Command Data		Command Data		
00000000 (0x00)	ACK	00000000 (0x00)	ACK	00000000 (0x00)	ACK	
Command Data		00000001 (0x01)	STOP			



Note 1: Local Dimming demo OFF



Note 2: Local Dimming demo ON



## A.2 I2C timing

Symbol	Parameter	Min.	Max.	Unit
$t_{\text{SU-STA}}$	Start setup time	250	-	ns
$t_{\text{HD-STA}}$	Start hold time	250	-	ns
$t_{\text{SU-DAT}}$	Data setup time	80	-	ns
$t_{\text{HD-DAT}}$	Data hold time	0	-	ns
$t_{\text{SU-STO}}$	Stop setup time	250	-	ns
$t_{\text{BUF}}$	Time between Stop condition and next Start condition	500	-	ns

